Amendments to the Claims

1. (*Currently Amended*) An electronic signal processing circuit, comprising:

[[-]] a plurality of chained stream processing circuits ~~(12a-d)~~, each having a stream input and a stream output, for inputting and outputting an input and output stream of successive sample values;

[[-]] linking multiplexing circuits ~~(16a-c)~~, each linking a respective pair of stream processing circuits ~~(12a-d)~~, each linking multiplexing circuit ~~(16a-c)~~ being individually switchable to a normal mode and to a replacement mode, the linking multiplexing circuit ~~(16a-c)~~, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits ~~(12a-d)~~ in the respective pair;

[[-]] a shareable communication structure ~~(14a-c)~~ coupled to the linking multiplexing circuits ~~(16a-c)~~, each linking multiplexing circuit ~~(16a-c)~~, when in the replacement mode, providing a continuous connection for supplying successive sample values from a second stream from the communication structure ~~(14a-c)~~ to a receiving one of the stream processing circuits ~~(12a-d)~~ in the respective pair of the linking multiplexing circuit ~~(16a-c)~~;

[[-]] a control circuit ~~(18)~~ coupled to the linking multiplexing circuits ~~(16a-c)~~, arranged to keep a selectable one of the multiplexing circuits ~~(16a-c)~~ in the replacement mode so that the selectable one of the linking multiplexing circuits ~~(16a-c)~~ passes a stream of successive sample from the second stream to the receiving one of the processing circuits in the respective pair of linking multiplexing circuit ~~(16a-c)~~, while keeping at least part of the other linking multiplexing circuits ~~(16a-c)~~ in the normal mode.

2. (*Currently Amended*) An electronic signal processing circuit according to claim 1, comprising interface circuits, each coupled between the communication structure ~~(14a-c)~~ and the stream output of a respective one of the stream processing circuits ~~(12a-d)~~, each interface circuits being individually switchable to an output mode under control of the control circuit (IS), each interface circuit, when in the output mode, passing successive

samples of the second stream or a further stream from the stream output of a respective one of the stream processing circuits ~~(12a-d)~~ to the communication structure.

3. (*Currently Amended*) An electronic signal processing circuit according to claim 2, wherein the communication structure comprises a plurality of chained multiplexing circuits ~~(14a-c)~~, individually controllable by the control circuit ~~(18)~~, each chained multiplexing circuit ~~(14a-c)~~ corresponding to a respective corresponding one of the stream processing circuits ~~(12a-d)~~, each having a first input, a second input and an output, the first input being coupled to the stream output of the corresponding one of the stream processing circuits ~~(12a-d)~~, the second input being coupled to the output of the chained multiplexing circuit ~~(12a-d)~~ that corresponds to a preceding one of the stream processing circuit ~~(12a-d)~~ whose stream output is linked to the corresponding one of the stream processing circuit ~~(12a-d)~~ by one of the multiplexing circuits ~~(16a-c)~~.

4. (*Currently Amended*) An electronic signal processing integrated circuit according to claim 3, wherein each linking multiplexing circuit ~~(16a-c)~~ has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits ~~(12a-d)~~ to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits ~~(16a-c)~~ that corresponds to the linked one of the stream processing circuits ~~(12a-d)~~.

5. (*Currently Amended*) An electronic signal processing circuit according to claim 3, wherein each linking multiplexing circuit ~~(16a-c)~~ has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits ~~(12a-d)~~, to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuit ~~(12a-d)~~ that corresponds to the preceding one of the stream processing circuits whose stream output is linked to the input of the linked one of the stream processing circuits ~~(12a-d)~~.

6. (*Currently Amended*) An electronic signal processing circuit according to claim 2, comprising a further plurality of chained stream processing circuits (~~12a-d~~), further linking multiplexing circuits (~~16a-e~~), a further shareable communication structure, mutually coupled as claimed for the first mentioned plurality of chained stream processing circuits (~~12a-e~~), linking multiplexing circuits (~~16a-e~~), and shareable communication structure, the electronic signal processing circuit furthermore comprising a router circuit (~~20~~) having a first, second and third input coupled to an output of the shareable communication structure, an output of the further shareable communication structure and a first external connection terminal (~~22~~) of the electronic signal processing circuit respectively, the router circuit (~~20~~) having a first, second and third output, coupled to an input of the shareable communication structure, an input of the further shareable communication structure and a second external connection terminal (~~24~~) of the electronic signal processing circuit respectively, the router circuit (~~20~~) being arranged to establish selectable connection patterns between its inputs and outputs under control of the control circuit (~~18~~).

7. (*Currently Amended*) An electronic signal processing circuit according to claim 6, wherein the plurality of stream processing circuits (~~12a-d~~) is a transmission pre-processing circuit, the stream processing circuits (~~12a-d~~) being arranged to perform respective chained functions in the encoding of data in a transmission signal, the plurality of further stream processing circuits (~~12a-d~~) being a reception postprocessing circuit, the further stream processing circuits (~~12a-d~~) being arranged to perform respective inverse functions of the chained functions to decode data from a received signal.

8. (*Original*) An electronic signal processing circuit according to claim 1, comprised on an integrated circuit chip.

9. (*Currently Amended*) A method of testing an electronic signal processing circuit (~~10~~) that comprises a plurality of stream processing circuits (~~12a-d~~) that are connected in a network which passes streams of sample values between pairs of the stream processing circuits (~~12a-d~~), the method comprising:

[[-]] providing a shareable communication structure coupled to stream inputs and outputs of the stream processing circuits ~~(12a-d)~~, the shareable communication structure being redundant during normal use of the electronic signal processing circuit ~~(10)~~;

[[-]] in a test mode, extracting output streams from selected normally internal stream processing circuits ~~(12a-d) and/or supplying~~ or supplying input streams to selected normally internal stream processing circuits via the shareable communication structure.